Solid State Phenomena Vols. 108-109 (2005) pp 77-82 *Online: 2005-12-15*

doi:10.4028/www.scientific.net/SSP.108-109.77

Carrier accumulation in silicon-on-insulator structures containing Ge nanocrystals in the burried SiO_2 layer

I. E. Tyschenko[a], A. A. Frantsuzov[b], O. V. Naumova[c], B. I. Fomin[d], D. V. Nikolaev[e], V. P. Popov[f]

Institute of Semiconductor Physics, Novosibirsk, 630090, Russia

[a]tys@isp.nsc.ru, [b]aa_fran@.isp.nsc.ru, [c]naumova@isp.nsc.ru, [d]fomin@thrmo.isp.nsc.ru,

[e]nikolaev@isp.nsc.ru, [f]popov@isp.nsc.ru

Keywords: Silicon-on-insulator, Germanium, Nanocrystals, Carrier trapping.

Abstract. Electro-physical properties of metal-oxide-silicon (MOS) structures and MOS transistors, prepared in the top silicon layer of silicon-on-insulator (SOI) structures containing Ge nanocrystals in the buried SiO_2 layers, have been studied. It was obtained that carrier accumulation in MOS structures depend on the direction of built-in electrical field in MOS structures. Accumulation of the excess negative charges in the case of p-channel transistors is associated with electron trapping on Ge nanocrystals synthesized in the buried dielectric. In the case of n-channel transistor, positive charge related to the Si/SiO_2 interface or to the charged oxide is accumulated. The Ge atoms diffused to the SiO_2/Si interface can stimulate the formation of the excess positive charge.

Introduction. Silicon and germanium nanocrystals synthesized in SiO_2 layers have been proposed for potential applications in scalable nonvolatile memory devices [1, 2]. In this paper, we report the effect of Ge nanocrystals, ion-beam synthesized in the buried silicon dioxide, on the electro-physical properties of MOS devices fabricated in the top silicon layer of SOI structure.

Experiment. To produce Ge nanocrystals, thermally grown 220 nm thick SiO_2 films were implanted with Ge^+ ions at an energy of 40 keV to a dose ranging from 5×10^{15} to 8×10^{15} cm^{-2} and then annealed at the temperature T_a of 800 ^oC for 0.5 h in an Ar ambient. As a result, Ge nanocrystals were synthesized in the top near-surface region. After that, silicon films were bonded upon the nanocrystal containing structure. Thus, SOI structures with the 600 nm thick top Si film and 220 nm thick buried SiO_2 layer containing Ge nanocrystals were produced. Finally, lateral p-n-p- (n-channel) and n-p-n- (p-channel) MOS transistors were formed in the top silicon film. The n^+- and p^+ active regions were produced by the ion implantation of B^+ and As^+ ions, respectively, with subsequent annealing at T_a = 1050 ^oC for 10 s. Polycrystalline silicon gates of the transistors were of the 0.5 μm length. Contacts to polycrystalline silicon gates and to the backside of the samples were produced by magnetron sputtering of Al. Figure 1 shows a schematic of the device structure. To measure the high-frequency capacitance-voltage (C-V) characteristics, a number of the structures had the Al contact electrodes adjoining to the n- or p-drain. Thus, vertical Al/n^+-Si/Ge-SiO_2/p-Si/Al and Al/p^+-Si/Ge-SiO_2/p-Si/Al structures were prepared. The high-frequency (1 MHz) C-V characteristics were measured with EDK-6817 meter using scan velocity of ~0.85 V/s. The drain-gate current-voltage (I-V) characteristics of the prepared MOS transistors were measured for injection time of 10 and 15 min. For comparison, the respective structures without Ge nanocrystals were also measured. Cross-sectional transmission electron microscopy (XTEM) and high-resolution electron microscopy (HREM) were employed for the structural control of the Ge nanocrystal containing SOI samples.

Results. Figure 2a displays an XTEM image of the SOI structure containing Ge nanocrystals near the top SiO_2/Si interface of the buried SiO_2 layer. An HREM image of Ge nanocrystals synthesized

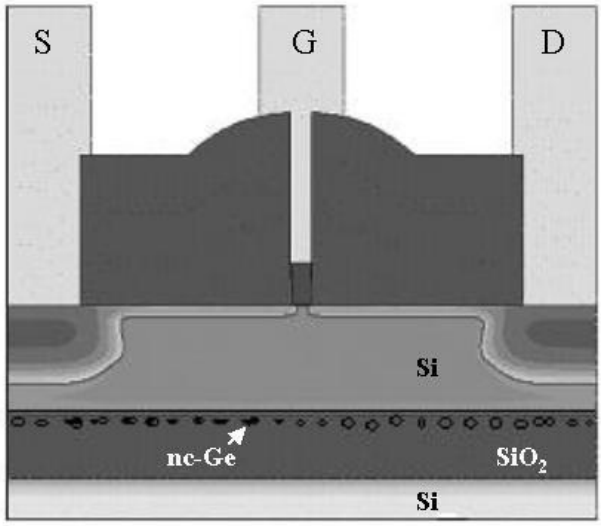
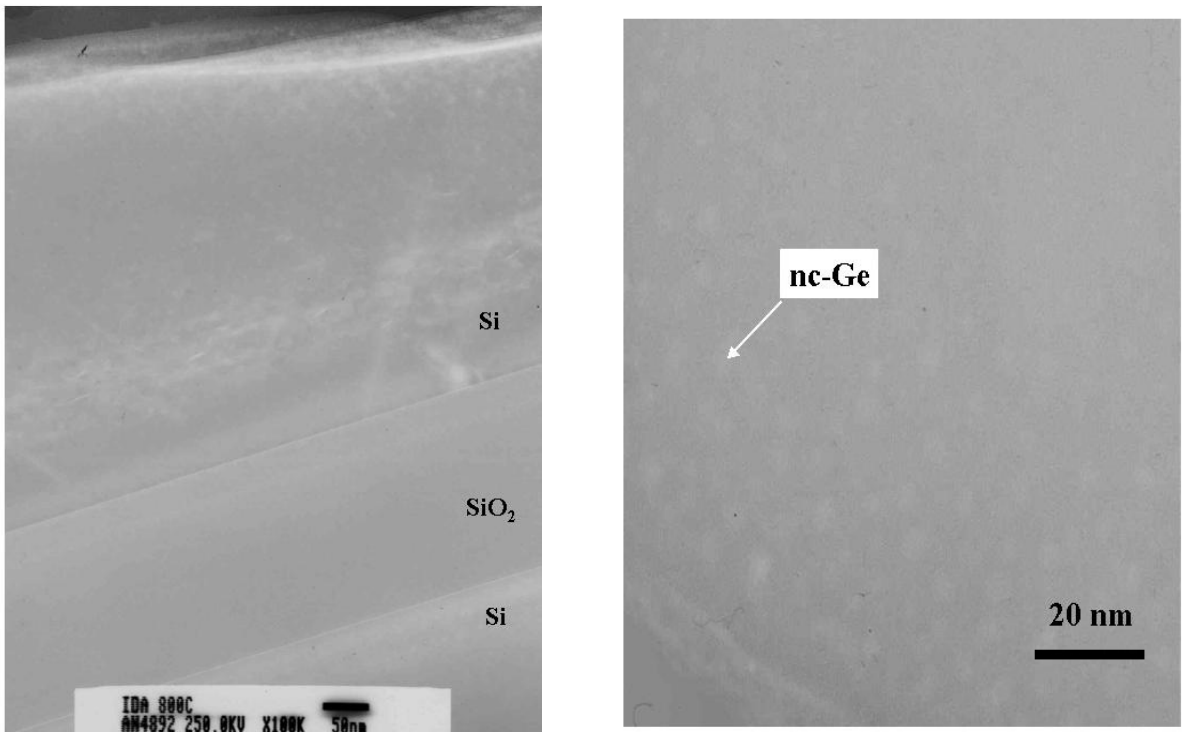


Figure 1. Schematic of the MOS devices prepared on the SOI structure containing Ge nanocrystals in the buried SiO_2 layer.



a) **b)**

Figure 2. (a) An XTEM image of the prepared SOI structure; **(b)** an HREM image of Ge nanocrystals synthesized in the buried SiO_2 layer of the SOI structure.

in the SiO_2 layer by Ge^+-ion implantation and subsequent annealing at T_a = 800 ^oC is shown in figure 2b. An average size of the nanocrystals was about 3-5 nm.

The influence of the back gate (substrate) bias V_{back} on the drain-gate I-V characteristics of the n-p-n transistors, based on the SOI structures with Ge nanocrystals, is summarized in Fig. 3. One can see that n-p-n transistor was already switched on by zero value of the back gate bias. That can be related to the accumulation of the positive charge either at the Si/SiO_2 interface or within the dioxide. The inset of Fig. 3 shows changing charge ΔQ, obtained from the flat-band voltage shift, as a function of the applied electric field E.

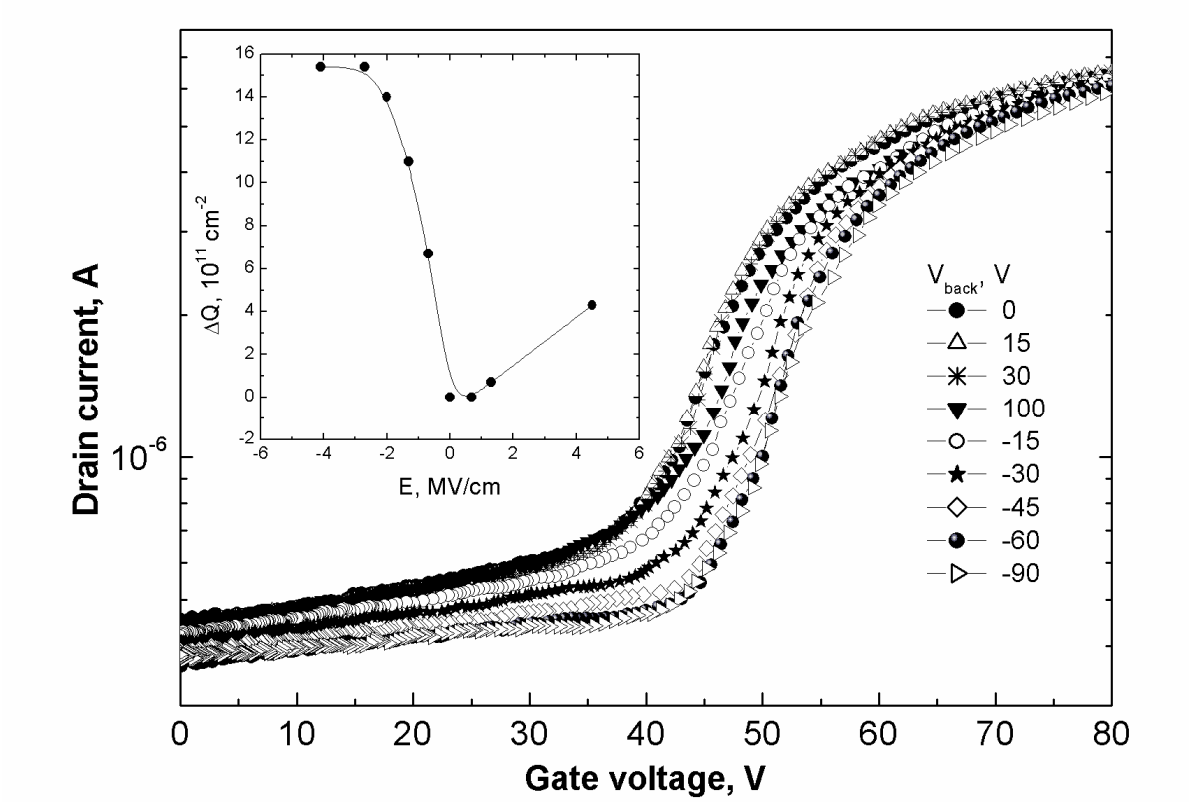


Figure 3. The drain-gate I-V characteristics of the n-p-n transistor, prepared in the top Si layer of the SOI structure containing Ge nanocrystals, as a function of the back gate (substrate) bias V_{back}. Duration of carrier injection from the substrate was t_{stress} = 10 min. The inset shows changing charge ΔQ in the system as a function of the applied electric field E.

Figure 4 displays the influence of V_{back} on the drain-gate I-V characteristics of the p-n-p (p-channel) transistor, based on the SOI structure with Ge nanocrystals. In this case, transistor was also switched on by the zero value of back gate bias. The formation of the negative charge in silicon dioxide is a possible reason of the observed effect. It is necessary to note, that negative charge in the SiO_2 film may be partially compensated by the positive charge at the Si/SiO_2 interface. The p-channel transistor was switched on at the back gate bias V_{back} = 100 V. Under these conditions, captured electrons compensated completely the positive charges. Total charge obtained from the shift of the flat band voltage as a function of the electric field is shown in the inset of Fig. 4. In this case, duration of carrier injection from the substrate was t_{stress} = 15 min.

The high-frequency C-V characteristics of both Al/n^+-Si/Ge-SiO_2/p-Si/Al (with the nanocrystals) and Al/n^+-$Si/SiO_2/p$-Si/Al (without the nanocrystals) structures are summarized in Fig. 5. The capacitance-voltage characteristics of the structure containing the Ge^+ ion implanted SiO_2 layer were shifted as compared to that from the structures with the unimplanted dioxide. The observed negative shift in the flat-band voltage corresponds to positive charge trapping in the dioxide. One can also see, that the C-V-characteristic slope obtained from first kind of the structures became smaller in comparison with that of the structures without germanium. That can be related

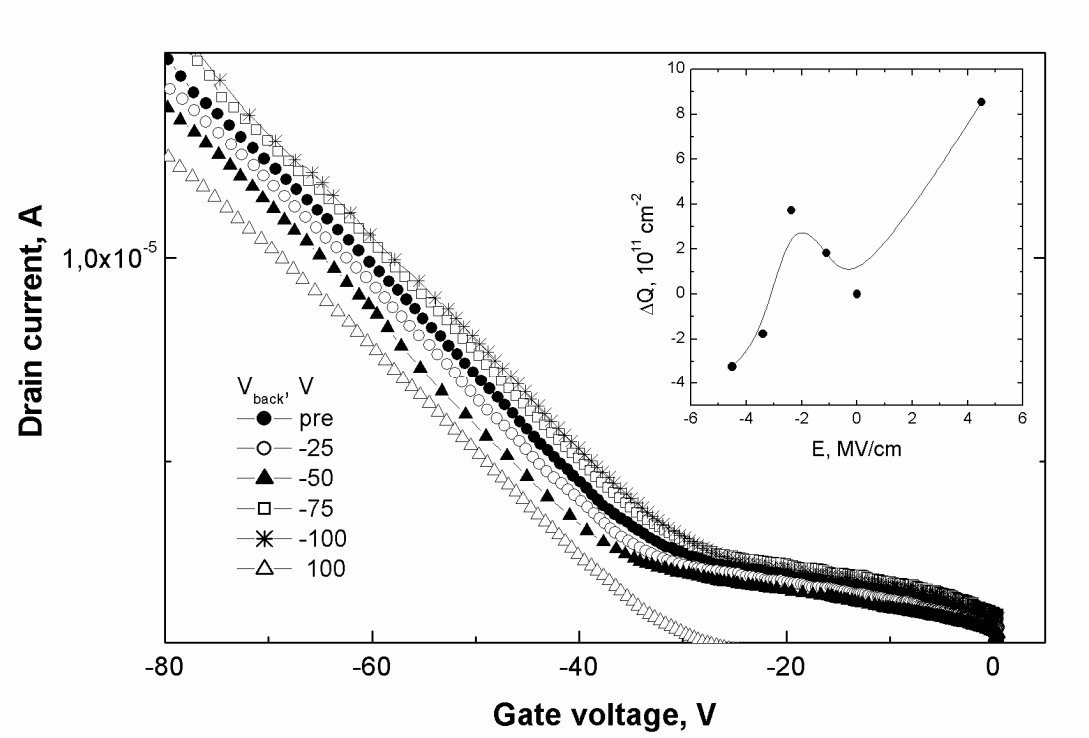


Figure 4. The drain-gate I-V characteristics of the p-n-p transistor, prepared in the top Si layer of the SOI structure containing Ge nanocrystals, as a function of the substrate bias V_{back}. Duration of carrier injection from the substrate was t_{stress} = 15 min. The inset shows changing charge in the system ΔQ as a function of the applied electric field E.

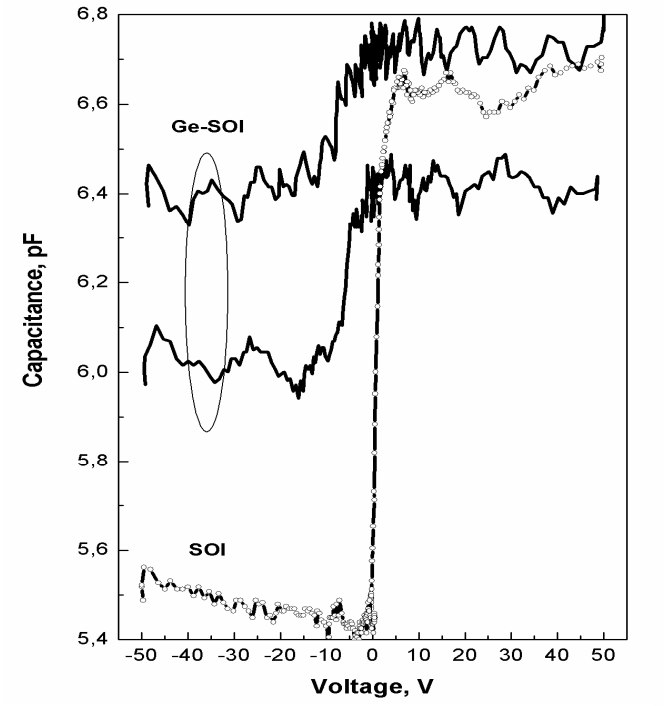


Figure 5. C-V characteristics of Al/n^+-Si/Ge-SiO_2/p-Si/Al (Ge-SOI) and Al/n^+-Si/SiO_2/p-Si/Al (SOI) structures.

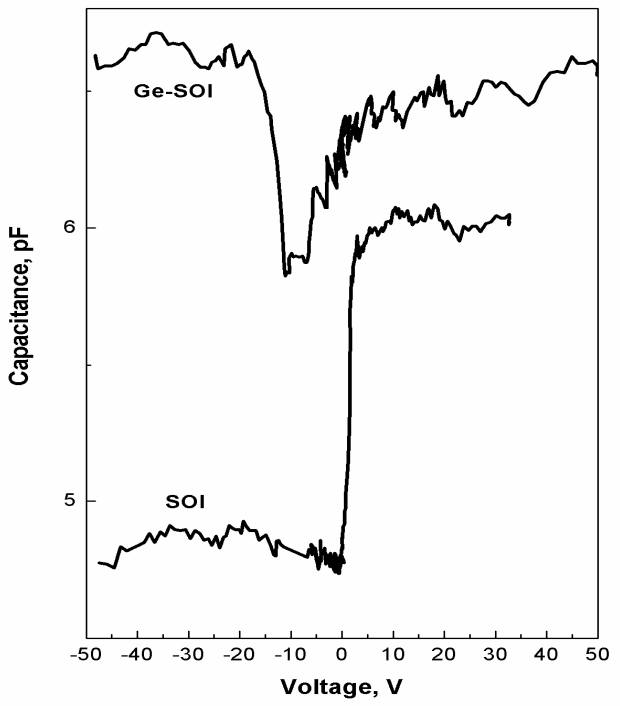


Figure 6. C-V characteristics of Al/p^+-Si/Ge-SiO_2/p-Si/Al (Ge-SOI) and Al/p^+-Si/SiO_2/p-Si/Al (SOI) structures.

to an increase in the surface state density at the Si/SiO_2 interface. The value of the accumulated positive charge of 7×10^{11} cm^{-2} was estimated from the flat-band voltage shift. This value is in good accordance with that obtained from the I-V drain-gate characteristics (see Fig. 3).

Fig. 6 shows the C-V characteristics of Al/p^+-Si/Ge-SiO_2/p-Si/Al and Al/p^+-$Si/SiO_2/p$-Si/Al structures. In this case, first, a negative shift in the flat-band voltage was also observed in C-V curve of the structures containing the Ge^+ ion implanted buried SiO_2 film as compared to that of the samples with unimplanted one. This shift in the flat-band voltage can be attributed to the positive charges near the Si/SiO_2 interface. Surprisingly, further increase of the negative voltage resulted in growing dielectric capacitance again. Trapping of the negative carriers by the Ge nanocrystals within the SiO_2 layer may be a possible reason of the observed effect.

From the results presented in Fig. 5 and Fig. 6, it is apparent that the change of the conductivity type of the top silicon region is sufficient to have an appreciable influence on the C-V characteristics of the Ge^+ ion implanted structures.

Discussion

The results above show that two kinds of the charge traps take place in the structures containing the Ge^+ ion implanted dioxide layer. To clear the nature of the formation of these charge traps, it is necessary to analyze the behavior of germanium atoms in the silicon dioxide during subsequent high-temperature annealing. Increasing T_a higher than 900 ^oC results in a diffusion of germanium atoms from the implanted region to the top surface and to the Si/SiO_2 interface [3, 4]. In the case of the bonded structures, a diffusion of Ge atoms may be dramatically enhanced by hydrogen penetrating into the ion-implanted SiO_2 film [4, 5]. This means that along with the nucleation of Ge nanocrystals within the SiO_2 matrix, the accumulation of Ge at the top Si/SiO_2 interface of SOI structure takes place. According to literature data [6], at that, the nanocrystals are the traps of the negative charges. Germanium atoms accumulated at the interface produce the traps of the positive charges. Therefore, the observed positive charge may be connected with the hole capture on the Ge centers at the Si/SiO_2 interface. The nature of these centers is not clear up to now. In accordance with the results obtained in reference [7], elemental Ge at the Si/SiO_2 interface could be responsible for deep level states in Si band gap. In this case, an interface state density is below the surface germanium concentration (in our experiments, the surface Ge concentration could be amount to about 10% of an ion dose, i.e. up to 8×10^{14} cm^{-2}). This concentration is much higher than the surface state density of the dangling bonds really observed in the MOS structures. Note, that the configurations of defects, produced by Si and Ge atoms, are identical ones. Therefore, a diffusion of germanium has not essentially to increase the state density at the Si/SiO_2 interface. There are two possible effects of Ge atoms on the surface state density. First, the defects, produced by Ge atoms, have energy out of the Si band gap, whereas energy levels of the Si binding defects are within the silicon band gap. Second, the bonds related to Ge atoms are weaker than the corresponding Si bonds. This can result in the increasing defect concentration near the interface.

Two kinds of the charge traps in Si/SiO_2 system allow explain the C-V characteristics measured from the structures with the top silicon of different conductivity types. The polarity of conductivity of the silicon layers determines the direction of the electrical field within the dielectric. Accordingly, filling of the respective states is limited by the build-in electric field.

Conclusion

Electro-physical properties of metal-oxide-silicon (MOS) structures and MOS transistors, prepared in the top silicon layer of silicon-on-insulator (SOI) structures containing Ge nanocrystals in the buried SiO_2 layers, have been studied. It was obtained that carrier accumulation in MOS structures depend on the direction of built-in electrical field in MOS structures. Accumulation of the excess negative charges in the case of p-channel transistors is associated with electron trapping on Ge nanocrystals synthesized in the buried dielectric. In the case of n-channel transistor, positive charge

related to the Si/SiO_2 interface or to the charged oxide is accumulated. The Ge atoms diffused to the SiO_2/Si interface can stimulate the formation of the excess positive charge.

Acknowledgment

The authors would like to thank Dr. I. I. Morosov for his help in the implantation of hydrogen ions.

References

[1] T. Gebel, L. rebohle, W. Skorupa, A. N. Nazarov, I. N. Osiyuk, V. S. Lysenko: Appl. Phys. Lett. Vol. 81 (2002), p. 2575.
[2] S. Huang, S. Baneriee, R. T. Tung, S. Oda: J. Appl. Phys. Vol. 93 (2003), p. 576.
[3] L. Rebohle, I. E. Tyschenko, J. von Borany, B. Schmidt, R. Grötzschel, A. Markwitz, R. A. Yankov, H. Fröb, W. Skorupa: Mater. Res. Soc. Symp. Proc. Vol. 486 (1998), p. 175.
[4] E. S. Marstein, A. E. Gunnæs, A. Olsen, T. G. Finstad, R. Turan, U. Serincan: J. Appl. Phys. Vol. 96 (2004), p. 4308.
[5] B. Schmidt, D. Crambole, F. Herrmann: Nucl. Instr. Meth. Phys. Res. B. Vol. 191 (2002), p. 482.
[6] A. N. Nazarov, T. Gebel, L. Rebohle, W. Skorupa, I. N. Osiyuk, V. S. Lysenko: J. Appl. Phys. Vol. 94 (2003), p. 4440.
[7] F. K. Goues, R. Rosenberg, T. Nguyen, F. Himpsel, B. S. Meyerson: J. Appl. Phys. Vol. 65 (1989), p. 1724.

Gettering and Defect Engineering in Semiconductor Technology XI
10.4028/www.scientific.net/SSP.108-109

Carrier Accumulation in Silicon-On-Insulator Structures Containing Ge Nanocrystals in the Burried SiO_2 Layer
10.4028/www.scientific.net/SSP.108-109.77

DOI References
[4] E. S. Marstein, A. E. Gunns, A. Olsen, T. G. Finstad, R. Turan, U. Serincan: J. Appl. Phys. Vol. 96 (2004), p. 4308.
doi:10.1063/1.1790579